Report on VLSI Design Review I

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1 Completed Work

- **Literature search:** we conducted literature search to identify the topic of our project, based on which we choose to work on priority encoder (PE) related topics due to its widely use in computer systems. A series of papers are found and analyzed to fully understand how PE designs were advanced and their performance improved in the past decade. The progress of PEs' development manifests that there are three major metrics in PE design, i.e., delay, power consumption and the number of transistors used, which will be our potential optimization objectives as well.
- **Specifying potential innovations:** 1) design a 8-bit PE with shorter delay, lower power dissipation or/and smaller number of transistors; 2) extract parasitic capacitances and resistances using Cadence and then derive formulas for delay and dynamic power consumption. 3) design a 32-bit or 64-bit PE with better delay performance.
- **Cadence Simulations:** we used Cadence to implement a CMOS PE based on active-low logic proposed in [1], which is able to achieve significant power saving with a small amount of transistors.

2 Remaining Tasks

2.1 Tasks Prior to the Proposal

Implement major PEs proposed in the cited papers, including a full parallel PE, two power-optimized PEs and an area-optimized PE. Then we will measure the metrics of delay, power consumption and the number of transistors using Cadence and NCSU_Devices_Free PDK45 library so that their performance can be evaluated and compared fairly in the same framework.

2.2 Tasks After the Proposal

- **8-bit PE design:** Based on the implementation of existed PEs using the same CMOS library, we plan to pinpoint their disadvantages and design a modified 8-bit PE to improve performance in terms of delay, power consumption or/and complexity.
- **Formula derivation:** By extracting parasitic capacitances and resistances of PEs using Cadence, we aim to deriving formulas for best- and worst-case propagation delays and power dissipation of a specific PEs. If the accuracy of the formulas could be validated through comparing with the results of simulations, then our work could be used as a

simple and quick approach to estimate PEs' performance metrics without conducting simulations.

- **64-bit PE design:** Design a power- or delay-optimized 64-bit PE with modified architecture to reduce power consumption or critical path delay. We also want to figure out whether a delay-optimized 8-bit PE could achieve optimal delay performance when applied to the design of a 64-bit PE.

Reference

[1] Preeti Panchal, C. Vinitha, Rashi Srivastava, P. Balasubramanian and N. E. Mastorakis, Design of 8-bit dynamic CMOS priority resolvers based on active-high and active-Low logic.